Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.129”**

**PAD FUNCTION:**

1. **GND**
2. **INPUT +**
3. **INPUT +**
4. **V –**
5. **BAL**
6. **BAL/STROBE**
7. **OUTPUT V +**

****

**Top Material: Al**

**Backside Material: TiNiAg**

**Bond Pad Size: .016” x .020” Gate**

**Backside Potential: DRAIN**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .045” X .056” DATE: 3/21/22**

**MFG: INT’L RECTIFIER THICKNESS .013” P/N: IRFR120Z**

**DG 10.1.2**

#### Rev B, 7/19/02